YUYANG WANG

800 S Harvard Blvd, Los Angeles, USA • (903) 215-2254 • yuyangwangeng@gmail.com
Personal Website: https://www.yuyangwangeng.com/

EDUCATION

Rochester Institute of Technology, Rochester — Aug., 2022 - May, 2024
Master of Science *- Computer Engineering, General* — **GPA:** 3.37

LeTourneau University, Longview, TX — Aug., 2017 - May, 2022
Bachelor of Science *- Electrical and Computer Engineering*
Minor *in Mathematics &* ***Minor*** *in Computer Science*

KEY SKILLS

- **Language:** C/C++, VHDL, Verilog, Python, Assembly, Matlab
- **Platform:** Cadence, Xilinx Vivado, Xilinx SDK, Quartus, FPGA, CPLD
- **Boards:** Nexys4 DDR, ZYBO Z7-20, STM32L476

RELEVANT COURSES

Machine Learning/Deep Learning/Robot Perception
Real-Time Embedded Systems
Reconfigurable Computing
Multiple Processor Systems

RESEARCH EXPERIENCE

Rochester Institute of Technology, Rochester, NY | Jan., 2024 – May, 2024
Evaluating Electro-Optical Frequency Mapping Attack Leakage in Integrated Circuits using Graph Neural Networks
- This work utilizes GNN to reduce the runtime of Electro-Optical Frequency Mapping attack leakage assessment in obfuscated circuits to rapidly identify candidate leaking nodes for further analysis
- Authors: Yuyang Wang, Cory Merkel, and Michael Zuzak [In preparation for publication]

ENGINEERING PROJECTS

Rochester Institute of Technology, Rochester, NY | Aug., 2022 – May, 2024
Embedded Systems - Signal Generation, Capture & Token Ring Project
- Developed a dual-channel I/O system for signal generation and capture with user-defined parameters.
- Supported isochronous DAC updates, noise addition, and analog signal digitization.
- Implemented RTOS queues and tasks for continuous user input.
- Integrated into a token ring communication system with message handling via serial interface.

Reconfigurable Computing & HW/SW Design for Crypto Apps
- Interfaced with PS2 keyboards, AXI Lite/Stream, and UART for data transfer using VHDL state machines and FIFOs.
- Developed a system for UART data transfer, DDR RAM read/write, and median filter operation on images.
- Implemented AES encryption/decryption across Zynq cores for secure data processing and display.

Digital IC Design - Binary Vector-Vector Multiplier with BIST
- Designed and built a vector-vector multiplier (dot product) for hardware accelerators.
- Included components: multiplier circuit, storage capability, and built-in self-test (BIST) module.
- Created a standard cells library for logic gates with schematic, layout, and simulation results.
- Verified hybrid design (parallel and serial input) using stimuli, Verilog testbench, and a golden signature.

LeTourneau University, Longview, TX | Aug., 2021 – May, 2022
Intro to Microprocessors/Microcomputers - Single Board Computer
- Designed schematic and PCB layout, sourced parts, soldered components, and troubleshooted with logic analyzer.
- Key components: Processor, CPU, CPLD, DUART, RAM, ROM, Driver.
- Configured pins using Quartus, coded CPLD in VHDL, and Motorola 68K chip in Assembly.
- Programmed a basic OS with functions: ASCII HEX to HEX, HEX to ASCII HEX, and S-Record reading.

INDUSTRY EXPERIENCE

Shanghai Keyang Technology Co. Ltd., Shanghai, China | July, 2020 – Dec., 2020
Engineering Intern
- Managed quality assurance for water monitoring devices, analyzed feedback for component checks on a 4-person team.
- Collected and organized data for in development product performance verification on a 2-person team.

AWARDS AND HONORS

Scholarships
- **RIT Graduate Scholarship** | Rochester Institute of Technology | Aug., 2022 - May., 2024
- **Founder's Scholarship** | Letourneau University | Aug., 2017 - May., 2022